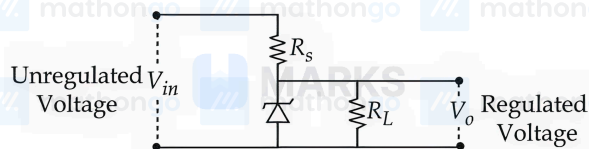


Q1. JEE Main 2026 (23 January Shift 1)

The following diagram shows a Zener diode as a voltage regulator. The Zener diode is rated at $V_z = 5\text{ V}$ and the desired current in load is 5 mA . The unregulated voltage source can supply upto 25 V . Considering the Zener diode can withstand four times of the load current, the value of resistor R_s (shown in circuit) should be _____ Ω .

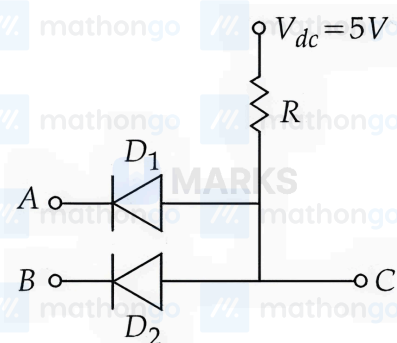


- (1) 100 (2) 1000
(3) 10 (4) None of the above

Q2. JEE Main 2026 (28 January Shift 2)

Two p-n junction diodes D_1 and D_2 are connected as shown in figure. A and B are input signals and C is the output.

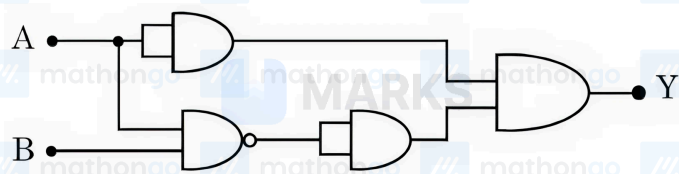
The given circuit will function as a _____.



- (1) NOR Gate (2) NAND Gate
(3) OR Gate (4) AND Gate

Q3. JEE Main 2026 (24 January Shift 2)

Identify the correct truth table of the given logic circuit.



(1)

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	0

(2)

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(3)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

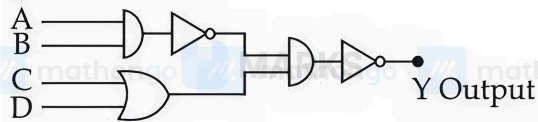
(4)

A	B	Y
0	0	0
0	1	0
1	0	1
1	1	0

Q4. JEE Main 2026 (22 January Shift 2)

The correct truth table for the given input data of the following logic gate is :

Inputs



(1)

A	B	C	D	Y
1	1	0	1	0
0	0	1	1	0
1	0	1	0	1
1	1	1	1	1

(3)

A	B	C	D	Y
1	1	0	1	1
0	0	1	1	0
1	0	1	0	0
1	1	1	1	1

(2)

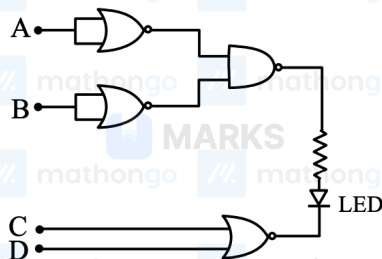
A	B	C	D	Y
1	1	0	1	0
0	0	1	1	1
1	0	1	0	1
1	1	1	1	1

(4)

A	B	C	D	Y
1	1	0	1	1
0	0	1	1	0
1	0	1	0	1
1	1	1	1	0

Q5. JEE Main 2026 (22 January Shift 1)

Find the correct combination of A, B, C and D inputs which can cause the LED to glow.



(1) 1101

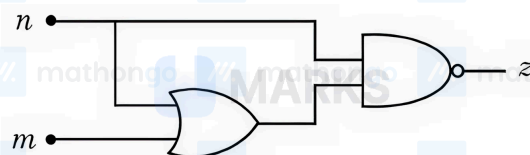
(2) 0011

(3) 1000

(4) 0100

Q6. JEE Main 2026 (23 January Shift 2)

For the given logic gate circuit, which of the following is the correct truth table?



(1)

n	m	z
0	0	0
0	1	1
1	1	0
1	0	1

(2)

n	m	z
0	0	1
0	1	0
1	1	1
1	0	0

(3)

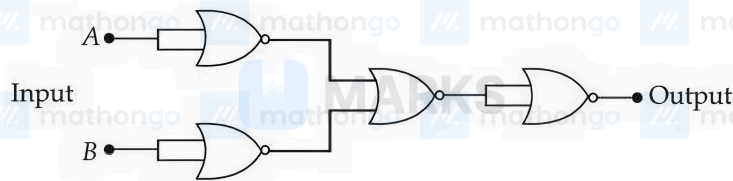
n	m	z
0	0	1
0	1	0
1	1	0
1	0	0

(4)

n	m	z
0	0	1
0	1	1
1	1	0
1	0	0

Q7. JEE Main 2026 (21 January Shift 1)

The given circuit works as :

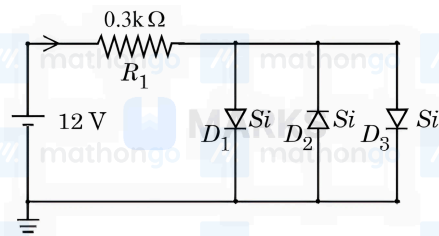


- (1) AND gate (2) NAND gate
(3) NOR gate (4) OR gate

Q8. JEE Main 2026 (28 January Shift 1)

Assuming in forward bias condition there is a voltage drop of 0.7 V across a silicon diode, the current through diode D_1 in the circuit is _____ mA.

(Assume all diodes in the given circuit are identical)



- (1) 17.6 (2) 18.8 (3) 11.7 (4) 20.15

Q9. JEE Main 2026 (24 January Shift 1)

A voltage regulating circuit consisting of Zener diode, having break-down voltage of 10 V and maximum power dissipation of 0.4 W, is operated at 15 V. The approximate value of protective resistance in this circuit is _____ Ω .

ANSWERS AND SOLUTIONS

1. (4) 2. (4) 3. (4) 4. (3) 5. (1) 6. (4) 7. (2) 8. (2)
9. 125

1. (4) This question has been dropped by NTA.

2. (4) If $A = 0$ and $B = 0$: Both diodes are forward biased. The potential at C is pulled down to approximately $0V$ (logic 0).

If $A = 0$ and $B = 1$: Diode D_1 is forward biased, pulling the potential at C down to $0V$ (logic 0). Diode D_2 is reverse biased.

If $A = 1$ and $B = 0$: Diode D_2 is forward biased, pulling the potential at C down to $0V$ (logic 0). Diode D_1 is reverse biased.

If $A = 1$ and $B = 1$: Both diodes are reverse biased. No current flows through the resistor R , so the potential at C remains at $V_{dc} = 5V$ (logic 1).

The truth table is:

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

This truth table corresponds to the AND gate logic operation $C = A \cdot B$.

Therefore, the circuit functions as an AND gate.

3. (4) Analysing the logic circuit:

The output is $Y = A \cdot \overline{A \cdot B}$

$$= A \cdot (\bar{A} + \bar{B})$$

$$= A\bar{A} + A\bar{B} = 0 + A\bar{B} = A\bar{B}$$

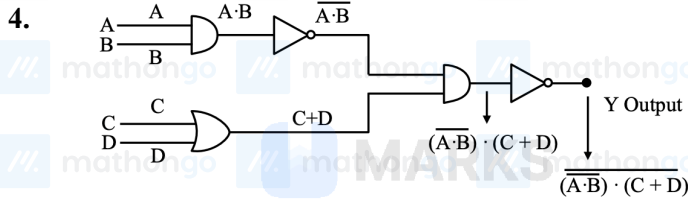
Truth table:

$$A = 0, B = 0 \Rightarrow Y = 0$$

$$A = 0, B = 1 \Rightarrow Y = 0$$

$$A = 1, B = 0 \Rightarrow Y = 1$$

$$A = 1, B = 1 \Rightarrow Y = 0$$



$$Y = \overline{(A \cdot B)} \cdot (C + D) = \overline{A \cdot B} + \overline{(C + D)}$$

$$Y = (A \cdot B) + \overline{(C + D)}$$

(3)

5. (1) The LED will glow if it is forward biased, which means the potential at the p-side must be higher than the potential at the n-side.

Let Y_1 be the output of the upper NAND gate (p-side) and Y_2 be the output of the lower NOR gate (n-side).

For the LED to glow, we need $Y_1 = 1$ and $Y_2 = 0$.

The upper circuit consists of two NOT gates (NOR gates with shorted inputs) followed by a NAND gate.

Output of first NOT gate is $\bar{A}$, and second is $\bar{B}$.

$$Y_1 = \overline{\bar{A} \cdot \bar{B}} = \bar{\bar{A}} + \bar{\bar{B}} = A + B \text{ (using De Morgan's Law).}$$

The lower circuit is a NOR gate with inputs C and D .

$$Y_2 = \overline{C + D}.$$

Condition 1: $Y_1 = 1 \implies A + B = 1$. This means at least one of A or B must be 1.

Condition 2: $Y_2 = 0 \implies \overline{C + D} = 0 \implies C + D = 1$. This means at least one of C or D must be 1.

Checking the options:

(1) $A = 1, B = 1, C = 0, D = 1$: $Y_1 = 1 + 1 = 1$ and $Y_2 = \overline{0 + 1} = 0$. (Satisfied)

(2) $A = 0, B = 0, C = 1, D = 1$: $Y_1 = 0 + 0 = 0$. (Not satisfied)

(3) $A = 1, B = 0, C = 0, D = 0$: $Y_2 = \overline{0 + 0} = 1$. (Not satisfied)

(4) $A = 0, B = 1, C = 0, D = 0$: $Y_2 = \overline{0 + 0} = 1$. (Not satisfied)

Thus, the correct combination is 1101.

6. (4) The given logic circuit consists of an OR gate and a NAND gate.

The output of the OR gate is $y = n + m$.

The inputs to the NAND gate are n and y .

The final output z is given by $z = \overline{n \cdot y} = \overline{n \cdot (n + m)}$.

Using Boolean algebra: $n \cdot (n + m) = n \cdot n + n \cdot m = n + n \cdot m = n(1 + m) = n$.

Therefore, $z = \bar{n}$.

Let's verify this with the truth table:

n	m	y = n + m	z = NAND(n, y)
0	0	0	1
0	1	1	1
1	1	1	0

1	0	1	0
---	---	---	---

Comparing this with the given options, option (4) matches the calculated truth table.

7. (2) Let the inputs be A and B. The circuit is composed of NOR gates.

A NOR gate with its inputs tied together acts as a NOT gate.

The output of the first NOR gate (input A) is $Y_1 = \overline{A + A} = \bar{A}$.

The output of the second NOR gate (input B) is $Y_2 = \overline{B + B} = \bar{B}$.

These outputs are fed into a third NOR gate. Its output is $Y_3 = \overline{Y_1 + Y_2} = \overline{\bar{A} + \bar{B}}$.

Using De Morgan's theorem, $Y_3 = \overline{(\bar{A}) \cdot (\bar{B})} = A \cdot B$.

This output Y_3 is the input to the fourth NOR gate, which is configured as a NOT gate.

The final output is $Y_{out} = \overline{Y_3} = \overline{A \cdot B}$.

The expression $\overline{A \cdot B}$ represents a NAND gate.

8. (2) $12 - 0.3 \times 10^3 I - 0.7 = 0$

$$\frac{11.3}{0.3 \times 10^3} = I$$

$$37.66 \times 10^{-3} \text{ A} = I$$

Current through diode D_1 , $I_1 = I/2$

$$I_1 = 18.83 \text{ mA}$$

9. (125) The maximum current through the Zener diode is determined by its maximum power dissipation:

$$I_{Z,max} = \frac{P_{max}}{V_Z} = \frac{0.4}{10} = 0.04 \text{ A}.$$

The protective series resistance must limit the current such that the Zener operates safely. Using Ohm's law across the series resistance and Zener when the Zener carries maximum current:

$$R_s = \frac{V_{in} - V_Z}{I_{Z,max}} = \frac{15 - 10}{0.04} = \frac{5}{0.04} = 125 \Omega$$